FEATURES

The CRSU-4x2488 is a single chip Clock Recovery and Synthesis Unit supporting four SONET/SDH links operating at 2488.32 Mbit/s.

- Processes four independent bit-serial 2488.32 Mbit/s STS-48 (STM-16) data streams with on-chip clock and data recovery and clock synthesis.
- Complies with Bellcore GR-253-CORE jitter tolerance, jitter transfer and intrinsic jitter criteria.
- Implements In-band Forward Error Correction (FEC) source and sink function according to ANSI Committee T1, Letter Ballot LB812.
- Implements In-band Forward Error Correction (FEC) line regeneration equipment (LRE) function according to ANSI Committee T1, Letter Ballot LB812.
- Provides performance monitoring of SONET Section, and Line layer entities or SDH Regenerator Section, and Multiplexer Section entities.
- Interfaces with downstream SONET/SDH framer devices over a set of four 4-bit, 622 MHz ports that conforms to the timing and AC characteristics defined in the Optical Internetworking Forum, contribution OIF-SF14-01.0.
- Supports line loop-back from the line side receive stream to the transmit stream and system side loop-back from the QSFI-4 transmit interface to the QSFI-4 receive stream interface.
- Supports loop-timing of the transmit stream from the associated receive stream.
- Supports Internal Channel-to-Channel loop Function. Channel 0 can be internally connected to Channel 1, and Channel 2 can be connected to Channel 3.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 1.8V CMOS core logic with 3.3V CMOS/TTL compatible digital inputs and digital outputs. PECL inputs and CML outputs are 3.3V compatible.
- Industrial temperature range (-40 °C to +85 °C Ambient, 125 °C Maximum Junction Temperature).

SONET SECTION AND LINE / SDH REGENERATOR AND MULTIPLEXER SECTION

- Frames to the SONET/SDH receive stream and inserts the framing bytes (A1, A2) into the transmit stream; unscrambles the received stream and scrambles the transmit stream.
- Calculates and compares the bit interleaved parity (BIP) error detection codes (B1, B2) for the receive stream. Calculates and inserts B1 in the transmit stream. Accumulates near end errors (B1, B2) and far end errors (M1).
- Extracts and filters the automatic protection switch (APS) channel (K1, K2) bytes into internal registers.
- Extracts and filters the synchronization status message (S1) byte into an internal register for the receive stream.
- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line remote defect indication (RDI-L), line alarm indication signal (AIS-L), and protection switching byte failure alarms on the receive stream.

580-pin 35 x 35 mm UPGA package.
Quad Clock Recovery and Synthesis Unit for 2488 Mbit/s

- Provides a mechanism to insert automatic line AIS insertion following detection of various received alarms LOS and LOF on to the QSFI-4 system side receive interface.
- Configurable to force Line AIS in the transmit stream.

SONET / SDH IN-BAND FORWARD ERROR CORRECTION
- Implements In-band Forward Error Correction sink function with a maximum delay of 15µs. Frames to the FEC status indication signal (FSI), and optionally outputs corrected data onto the receive system side interface.
- Counts corrected FEC errors in a set of software readable registers.

- Implements In-band Forward Error Correction source function with a maximum delay of 15µs. Optionally inserts FEC checksum bytes and FSI into the transmit stream. Line BIP (B2) bytes are compensated for the inserted FEC byte values.
- Support FEC Line Regeneration Equipment function with a maximum delay of 15.36µs by looping the receive stream to the transmit stream after FEC error correction.

APPLICATIONS
- Multi-Service Provisioning Platforms (MSPPs).
- SONET/SDH Add-Drop Multiplexers (ADMs).
- Digital Cross-Connects (DXCs).
- Optical Cross-Connects (OXC).
- Core IP Routers.
- Core Multi-Service Switches.
- Dense Wavelength Division Multiplexing (DWDM) Equipment.
- Coarse Wavelength Division Multiplexing (CWDM) Equipment.
- Compatible with OIF-standard 622 MHz interfaces such as those found in the following PMC-Sierra devices:
  - PM5324 ARROW-1x192.
  - PM5326 ARROW-2x192.
  - PM5317 SPECTRA-9953.
  - PM5390 S/UNI-9953.
  - PM5392 S/UNI-9953-POS.

JITTER PERFORMANCE

<table>
<thead>
<tr>
<th>Jitter Generation</th>
<th>PM5395 CRSU-4x2488</th>
<th>GR-253 Specification</th>
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<tbody>
<tr>
<td>Peak to Peak</td>
<td>0.075 UI</td>
<td>0.10 UI</td>
</tr>
<tr>
<td>RMS</td>
<td>0.005 UI</td>
<td>0.01 UI</td>
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</table>

Typical Application

QUAD OC-48 SONET/SDH ADM LINE CARD

- 2.48 Gbit/s Serial
- Quad SFI-4 (4 x 4-bit x 622 MHz)

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